16路LED驱动器和GPIO控制器

16-CHANNEL LED DRIVER AND GPIO CONTROLLER

■ FEATURES

- 16 multi-function I/O, each for LED drive (current-source dimming) or GPIO mode
- 256 steps linear dimming in LED drive mode
- Any GPIO can be configured as an input or an output independently
- Support interrupt, 8μs deglitch, low-level active
- Standard I^2C interface, AD1/AD0 select I^2C device address
- SDA, SCL, RSTN, and all GPIO can accept in 1.8V logic input
- Supply shutdown function, low-level active
- 2.5V~5.5V power supply
- Pb-free Packages, QFN4×4-24L

- 16个多功能IO，支持GPIO模式或LED驱动（电流源调光）
- LED驱动模式下256阶线性调光
- 任意GPIO可配置为独立的输入或输出
- 中断功能，8μs防抖，低电平有效
- 标准I^2C接口，AD1/AD0选择I^2C器件地址
- SDA, SCL, RSTN以及所有GPIO均支持1.8V逻辑电平
- 具有关断模式，低电平有效
- 2.5V~5.5V供电
- QFN4×4-24L，无铅封装

■ APPLICATIONS

- Cell Phone
- PDA/MP3/MP4/CD/Mini display

- 手机
- PDA/MP3/MP4/CD/迷你显示器显示

■ DESCRIPTION

HTR3316 is a 16 multi-function LED driver and GPIO controller. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I^2C device address selection inputs, AD0 and AD1. All I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When HTR3316 reads GPIO state through the I^2C interface, the interrupt is cleared. Interrupt has 8μs deglitch.

When the I/O ports are configured as LED drive mode, HTR3216 can set the current of LED drive between 0~I_{MAX} by I^2C interface, which is divided by 256 steps linear dimming. The default maximum current (I_{MAX}) is 37mA, and I_{MAX} can be changed in GCR register.

HTR3316 is available in QFN4×4-24L package, and 2.5V~5.5V power supply.

HTR3316是一款16路多功能LED驱动器和GPIO控制器。16个I/O端口中的任何一个都可以配置为LED驱动器模式或GPIO模式。此外，任何GPIO都可以单独配置为输入或输出。

通电后，所有16个I/O端口配置为默认GPIO输出，默认状态根据I^2C器件地址选择脚AD0和AD1设置。所有配置为输入的I/O端口都会持续监控状态变化。状态更改由INTN输出指示。当THR3316通过I^2C接口读取GPIO状态时，中断被清除。中断防抖时间为8μs。

当I/O端口配置为LED驱动器模式时，HTR3216可以通过I^2C接口将LED驱动器的电流设置在0~I_{MAX}之间，并可以该值除以256步进行线性调光。默认最大电流（I_{MAX}）为37mA，可在GCR寄存器中更改I_{MAX}。

HTR3316提供QFN4×4-24L封装，支持2.5V~5.5V电源。

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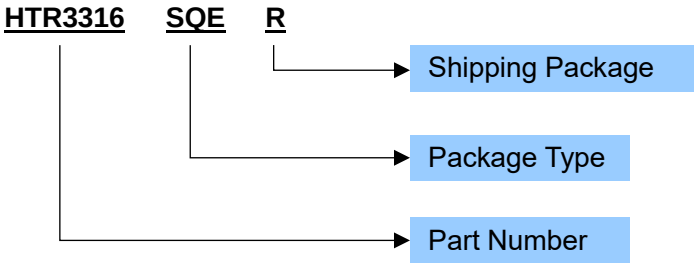
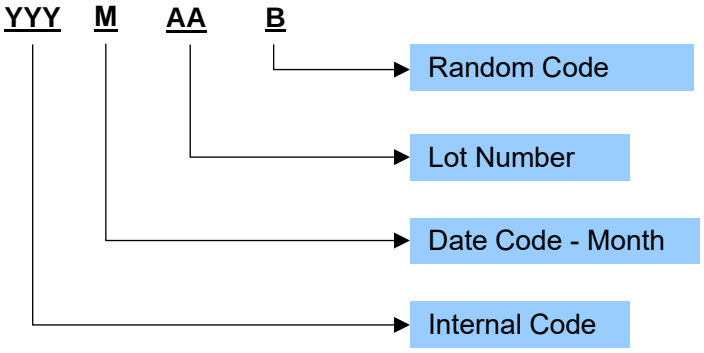
■ ORDERING INFORMATION

Ordering Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HTR3316SQER	QFN4×4-24L (SQE)	HTR3316 YYYMAAB[1]	-40℃～85℃	Tape and Reel (R) 5000PCS

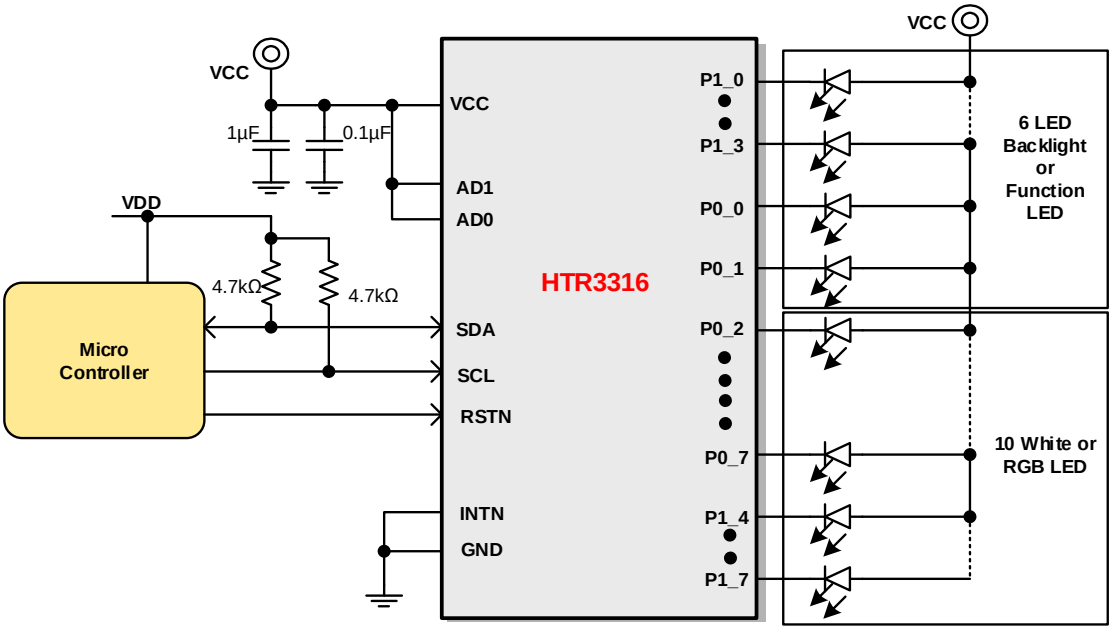
Ordering Number



Production Tracking Code



■ TYPICAL APPLICATION



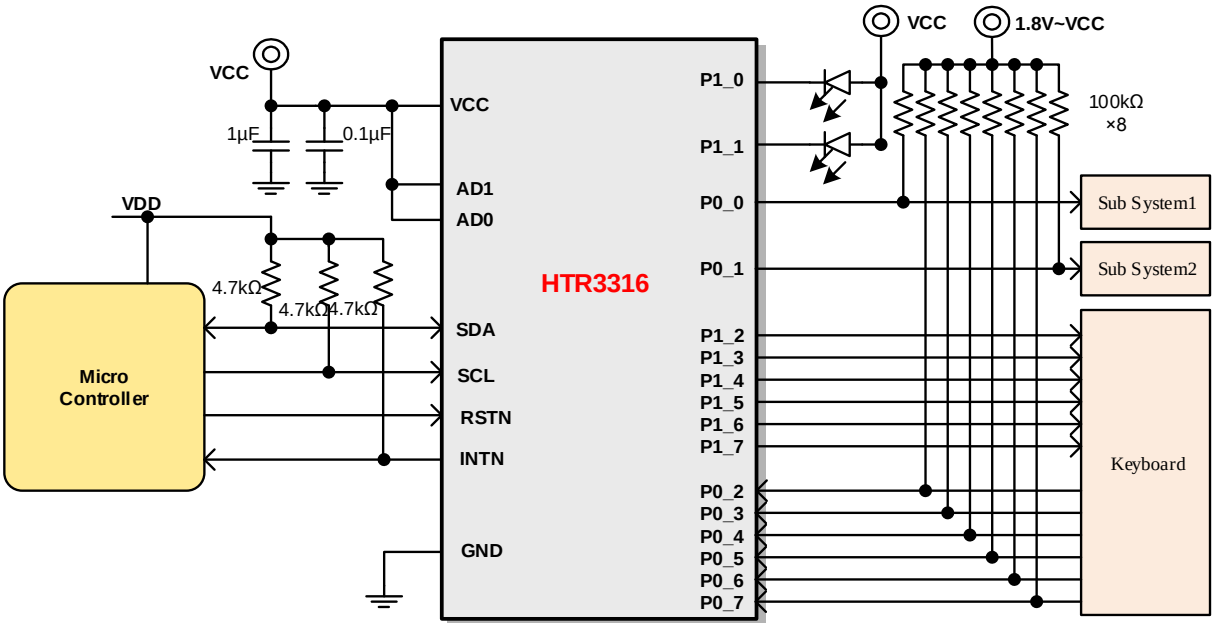
Drive 16 function LED, including 6 ports feasible for LED backlight

When LED anode is connected to VCC, the AD1/AD0 PIN must be connected to VCC to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

The Dropout performance of the low 6 LED Ports (P1_0~P1_3, P0_0~P0_1) is optimized, so these ports are recommended if you want to use HTR3316 to drive LED backlight。

当LED的阳极接VCC时，需将芯片的AD1/AD0接VCC，确保GPIO的上电默认状态为高或高阻，LED不会错误点亮。GPIO的上电默认状态由AD1/AD0的电平决定，具体参看表1。

低6路（P1_0~P1_3，P0_0~P0_1）的Dropout性能做了强化，在驱动LCD背光时建议选取这几路。



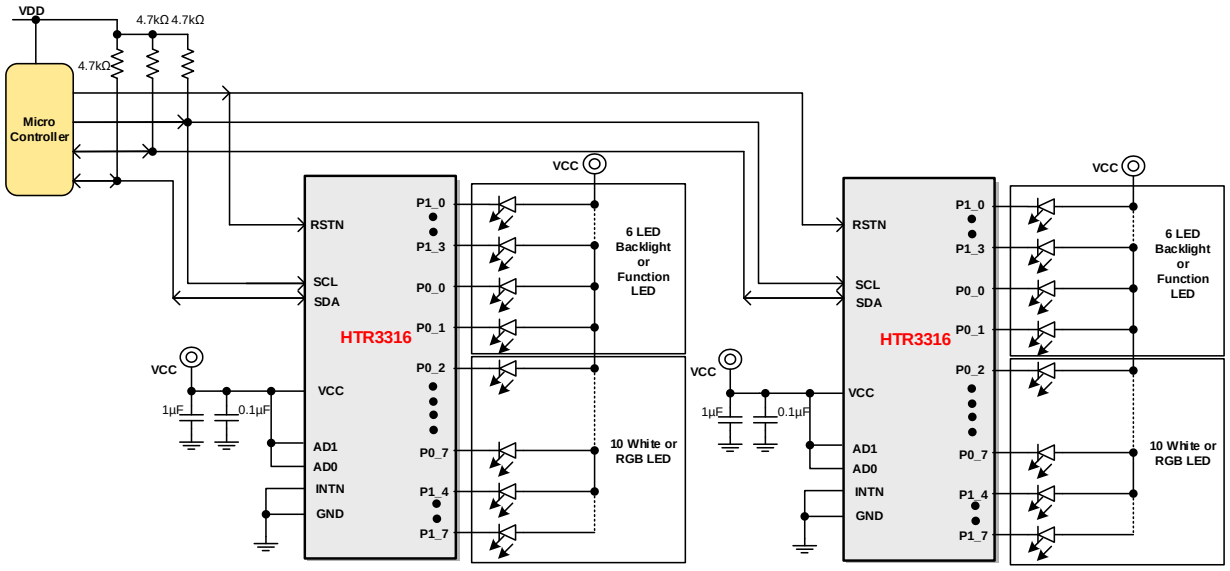
Function LED + keyboard/IO Extended

When LED anode is connected to VCC, the AD1/AD0 PIN must be connected to VCC to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. In the above application schematic, P1_0 and P1_1 are configured as LED mode, P0_0, P0_1 is configured as GPIO output to control sub system, P1_2~P1_7 are configured as GPIO output to drive the row line of keyboard, P0_2~P0_7 are configured as GPIO input to drive the column line of keyboard

当LED的阳极接VCC时，需将芯片的AD1/AD0接VBAT，确保GPIO的上电默认状态为高或高阻，LED不会错误点亮。GPIO的上电默认状态 由AD1/AD0的电平决定，具体参看表1。

16 路 IO 均可做 GPIO 或 LED 驱动使用。在图示的应用中，P1_0，P1_1 配置为 LED 模式，P0_0 配置为 GPIO 输出模式用来控制子系统， P1_2~P1_7 配置为 GPIO 输出模式用来驱动键盘的行线，P0_1~P0_7 配置为 GPIO 输入模式用来驱动键盘的列线。



Function LED + keyboard/IO Extended

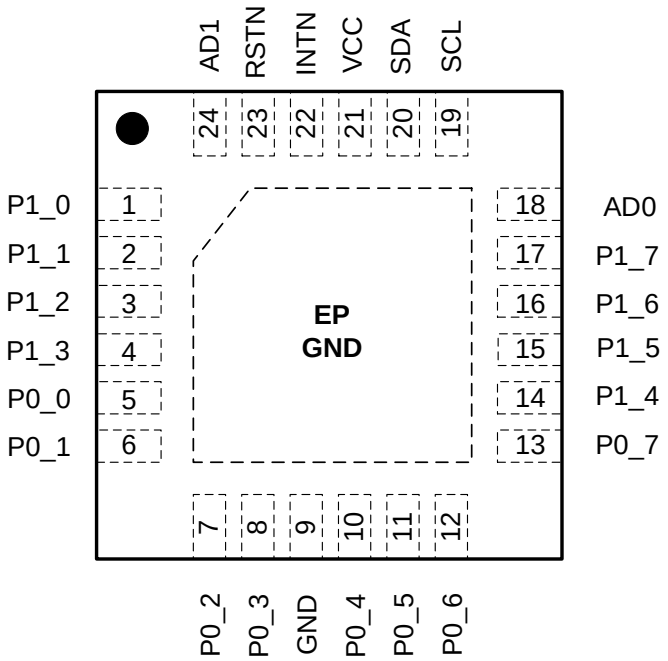
When LED anode is connected to VCC, the AD1/AD0 PIN must be connected to VCC to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

The 2 HTR3316s can share reset line RSTN and clock line SCL, but the data line SDA need to separate. So the 2 HTR3316s consume 4 GPIOs

当LED的阳极接VCC时，需将芯片的AD1/AD0接VCC，确保GPIO的上电默认状态为高或高阻，LED不会错误点亮。GPIO的上电默认状态 由AD1/AD0的电平决定，具体参看表1。

两颗HTR3316可复用复位线RSTN和时钟线SCL，数据线SDA需分开。总共需要4个GPIO口控制。

■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

Terminal No.	Name	Description
1~4	P1_0~P1_3	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN. 默认GPIO，输入或输出，推挽结构。可设置为LED驱动。上电默认状态与AD1/AD0相关。
5~8	P0_0~P0_3	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN. 默认GPIO，输入或输出，开漏结构（默认）或推挽结构。可设置为LED驱动。上电默认状态与AD1/AD0相关。
9	GND	Ground. 地
10~13	P0_4~P0_7	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN. 默认GPIO，输入或输出，开漏结构（默认）或推挽结构。可设置为LED驱动。上电默认状态与AD1/AD0相关。
14~17	P1_4~P1_7	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN. 默认GPIO，输入或输出，推挽结构。可设置为LED驱动。上电默认状态与AD1/AD0相关。
18	AD0	I^2C interface device address, connect to VCC or GND，and control the default state of output pin (refer to table 1)。 I^2C器件地址选择，接VCC或GND，并设置GPIO状态（见表1）。
19	SCL	I^2C serial clock. I^2C时钟
20	SDA	I^2C serial data. I^2C数据
21	VCC	Power supply. 电源输入端.
22	INTN	Interrupt output pin, open-drain mode, need external pull-up resistor; interrupt low active.

		中断输出，开漏结构，需外部上拉电阻；低有效
23	RSTN	Hardware reset pin, low reset; it has an internal 100 kΩ(typical) pull-low resistor. 硬件复位，低为复位；内部下拉100 kΩ（典型值）电阻
24	AD1	I^2C interface device address, connect to VCC or GND，and control the default state of output pin (refer to table 1)。 I^2C器件地址选择，接VCC或GND，并设置GPIO状态（见表1）。
EP	Exposed Thermal Pad, also GND	Ground. 地。

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for VCC	VCC	-0.3		6	V
Voltage at SCL, SDA, AD0, AD1, INTN, RSTN, P0_0~P0_7, P1_0~P1_7	V_{IO}	-0.3		VCC	V
Max power @ T_A = 25℃	P_{DMAX}		3.2		W
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-40		85	℃
Junction Temperature	T_J			150	℃
Storage Temperature	T_{STG}	-65		150	℃
Lead Temperature (Soldering 10 senconds)	T_{LEAD}		260		℃
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard)	θ_{JA}		31		°C/W
ESD (HBM)			±2		kV
ESD (CDM)			±1		kV

● Main Electrical Characteristics

Condition: T_A = 25°C, VCC = 3.6V, unless otherwise specified

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage and current						
Power supply voltage for VCC	VCC		2.5		5.5	V
Shutdown current	I_{SD}	RSTN=GND		0.1		uA
LED Driver						
Max current of LED drive	I_{MAX}	Configure DIMx Reg. as FFH		37		mA
Dropout voltage on low 6 ports (P1-0~P1_3, P0_0~P0_1)	V_{drop1}	I_{OUT}= 20mA		60		mV
Dropout voltage on high 10 ports (P0-2~P0_7, P1_4~P1_7)	V_{drop2}	I_{OUT}=20mA		80		mA
Digital pin output						
High-level output voltage (P0_7~P0_0, P1_7~P1_0)	V_{OH}	V_{CC}=2.5V，I_{SOURCE}=10mA		VCC-170		mV
		V_{CC}=3.6V，I_{SOURCE}=20mA		VCC-250		mV
		V_{CC}=5V，I_{SOURCE}=20mA		VCC-200		mV
Low-level output voltage (P0_7~P0_0, P1_7~P1_0)	V_{OL}	V_{CC}=2.5V，I_{SINK}=10mA		90		mV
		V_{CC}=3.6V，I_{SINK} =20mA		70		mV
		V_{CC}=5V，I_{SINK} =20mA		60		mV
Low-level output voltage (SDA, INTN)	V_{OL}	V_{CC}=2.5V，I_{SINK} =6mA		150		mV
		V_{CC}=3.6V，I_{SINK} =6mA		100		mV
		V_{CC}=5V，I_{SINK} =6mA		75		mV
Digital pin input						
High-level input voltage	V_{IH}	SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0	1.4			V
Low-level input voltage	V_{IL}				0.4	V
Input Current	I_I	SCL, SDA, RSTN, AD0, AD1, P0_7~P0_0, P1_7~P1_0, V_I = VCC or GND	-0.2		+0.2	uA
Input Capacitance	C_I			3		pF
Internal pull-low resistor in RSTN PIN	R_{RSTN}	Internal pull-low resistor in RSTN PIN		100k		Ω
Pulse width that RSTN	t_{SP_RSTN}	RSTN=VCC		10		us

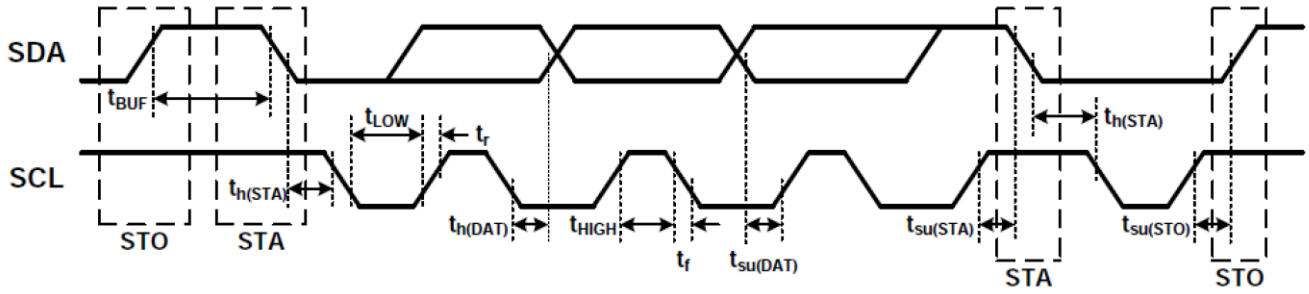
[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

PIN can filter						

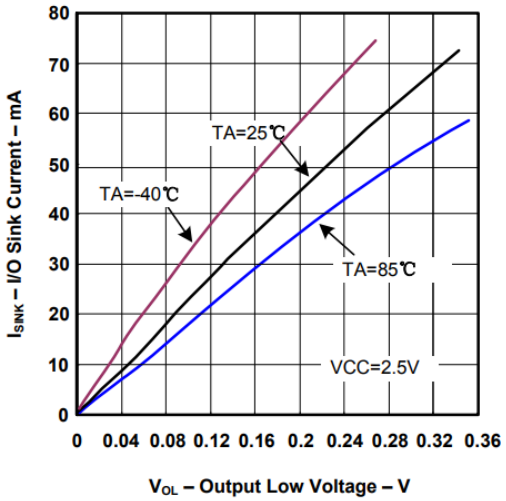
● I²C Control Port

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Serial-Clock frequency	f_{SCL}			400	kHz
Bus free time between a STOP and a START condition	t_{BUF}	1.3			us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	0.6			us
Setup time for a repeated START condition	$t_{su(STA)}$	0.6			us
Setup Time for SCL to STOP condition	$t_{su(STO)}$	0.6			us
Data hold time	$t_{h(DAT)}$	0		0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	100			ns
Required Pulse Duration, SCL HIGH	t_{HIGH}	0.7			us
Required Pulse Duration, SCL LOW	t_{LOW}	1.3			us
Rise Time, SCL and SDA	T_r			300	ns
Fall Time, SCL and SDA	T_f			300	ns

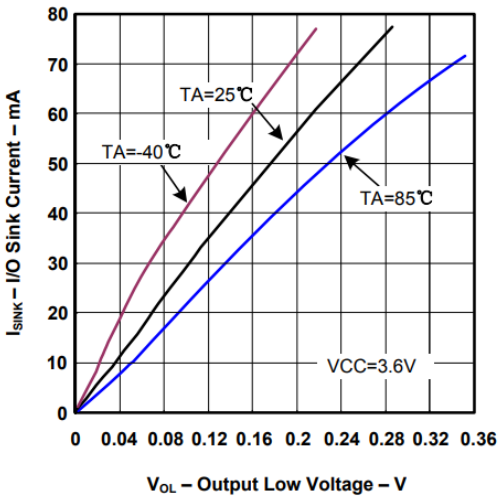


■ TYPICAL OPERATING CHARACTERISTICS

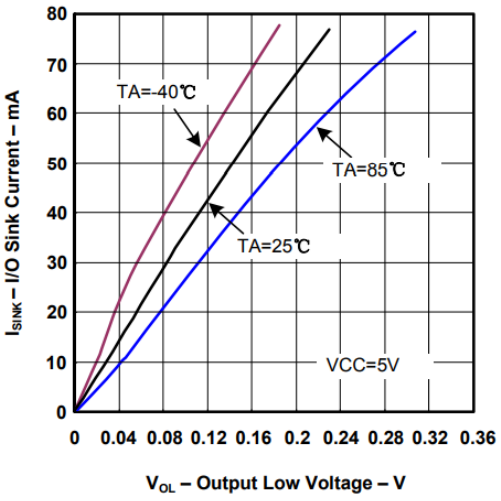
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



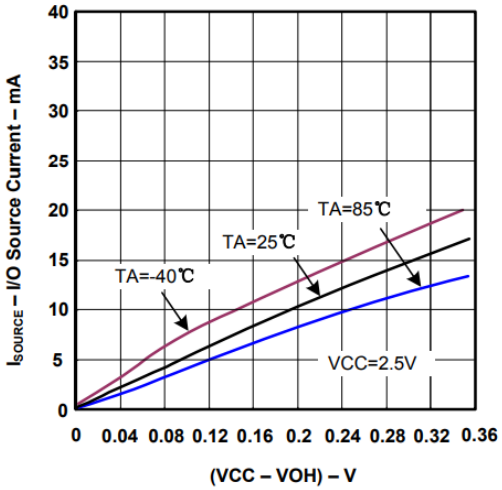
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



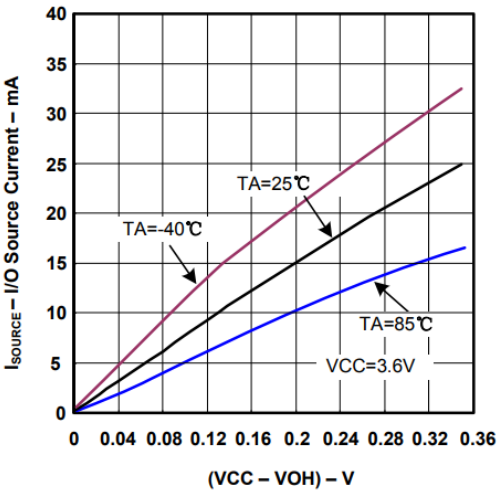
GPIO SINK CURRENT vs OUTPUT LOW VOLTAGE



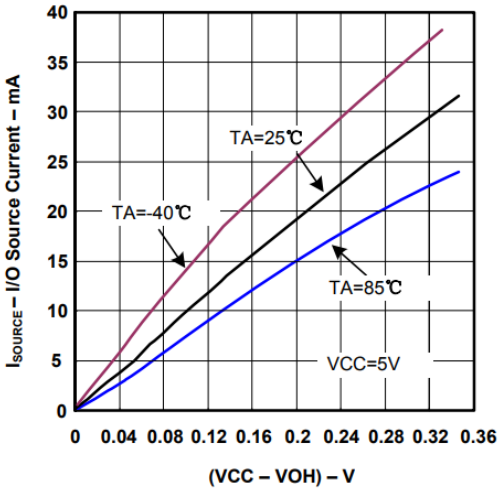
GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



GPIO SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



■ APPLICATION INFORMATION

HTR3316 is a 16 multi-function IO controller, which is applied for LED drive or GPIO. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

When configured as GPIO mode, all I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When THR3316 read GPIO state through the I2C interface, the interrupt is cleared.

When configured as LED drive, drive current range is 0~I_{MAX}, which 256 steps is divided. Default I_{MAX} is 37mA, and it can be changed in GCR register.

HTR3316是一款I2C接口、16 路呼吸灯及16 路扩展 GPIO 控制器，它包含 16 路双向GPIO端口，其中每路可通过指令配置为 LED驱动模式。在 GPIO 模式下，每一路 GPIO可单独配置为输入或输出。

当配置为GPIO模式时，所有配置为输入的I/O端口都会持续监控状态变化。状态更改由INTN输出指示。当THR3316通过I2C接口读取GPIO状态时，中断被清除。

配置为LED驱动时，驱动电流范围为0~I_{MAX}，分为256步。默认I_{MAX}为37mA，可在GCR寄存器中更改。

1 Power On

After power-up, about 100μs delay is required before RSTN set to high, otherwise, the device may work incorrectly. The minimal wait time for I2C communication is 5ms, during this period, some internal modules (such as LDO) start to work and reach a stable state.

Below is the recommended operation timing.

通电后，RSTN设置为高之前需要大约100μs的延迟，否则，设备可能无法正常工作。I2C通信的最短等待时间为5ms，在此期间，一些内部模块（如LDO）开始工作并达到稳定状态。

以下是建议的时序。

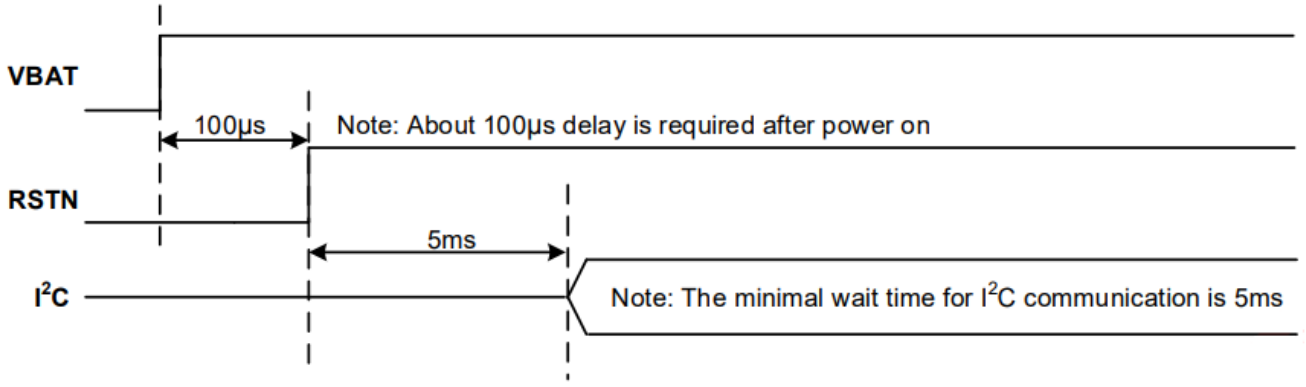


Figure 1 Power On Timing

2 GPIO OUTPUT

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I2C slave address selection inputs, AD0 and AD1, refer to table 1 for detail. The P1 port is Push-Pull mode; P0 port is Open-Drain mode (default) and can be configured as Push-Pull mode. When P0 port is Open-Drain mode, it need pull-up resistor.

上电后，16 路 GPIO 口默认为 GPIO 模式，且为输出状态，其输出默认值可通过 2 位器件地址（AD1、AD0）进行配置，具体配置方式见表 1。P1 端口为 Push-Pull 驱动；P0 端口默认为 Open-Drain 驱动，可通过配置全局控制寄存器设定为 Push-Pull 驱动。当 P0 口为 Open-Drain 模式时，需外接上拉电阻。

Table1 Default State of IO ports, AD1/AD0 and P0_x/P1_x

AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

3 GPIO INPUT/OUTPUT DIRECTION SELECT

The register Config_Port0 and Config_Port1 can configure a port as input or output. Each bit of the register is corresponding to each port, the bit set '1' as input, '0' as output. The default value is '0' as output.

Config_Port0 和 Config_Port 1 设定端口为输入、输出状态。寄存器每一位对应某个 GPIO 端口，该位置 '1' 代表输入状态，置 '0' 代表输出状态。默认值为 0，输出状态。

4 GPIO INPUT

User can get the current state of GPIO through reading the register Input_Port0 and Input_Port1 by I2C Interface. HTR3316B GPIO support 1.8V logic input.

通过 I2C 接口读 Input_Port0 和 Input_Port1 可获得当前 GPIO 端口逻辑状态。HTR3316B GPIO 口支持 1.8V 逻辑输入。

5 INTERRUPT

HTR3316B can monitor IO state to generate interrupt when configure port as GPI and GPIO interrupt enabled. External MCU is required acknowledge by INTN pin. INTN is open-drain output, low-level active, and need external pull-up resistor.

When HTR3316B detect port change, any input state from high-level to low-level or from low-level to high-level will generate interrupt after 8us internal deglitch. External MCU read GPIO_INPUT_A/B register to clear interrupt. P1 port state change must clear interrupt by read GPIO_INPUT_B register; P0 port state change must clear interrupt by read GPIO_INPUT_A register.

GPIO 口配置成输入模式，且使能中断功能后，其输入状态的变化可引起中断输出（INTN）的改变，从而向处理器提交中断请求。通过 I2C 接口读取 GPIO 输入状态时，可以清除中断。默认情况下，16 路 GPIO 口中断使能。HTR3316B 时刻监测输入状态，当检测到 GPIO 口逻辑电平变化，内部电路先进行 8μs 去抖动处理；若 8μs 后，确认其状态变化，则中断引脚电平拉低。不论 GPIO 口电平由低变高或由高变低，均能产生中断。将某一路 GPIO 口配置成输出模式、或关闭其中断使能后，则其状态的变化不会产生中断。

通过读取 Input_Port0 和 Input_Port1 寄存器可以清除中断，从而中断引脚通过外部上拉电阻拉高。由 P0 口变化产生的中断，必须读 Input_Port0 寄存器清除；由 P1 口变化产生的中断，必须读 Input_Port1 寄存器清除，不可跨组清除中断。中断清除时间点与 I2C 接口之间的关系见图 2。

当 GPIO 口状态变化产生中断后，改变其输入、输出状态或关闭该 IO 口中断使能，都不会清除中断；直至通过 I2C 接口读才能清除中断，或通过复位功能清除中断。

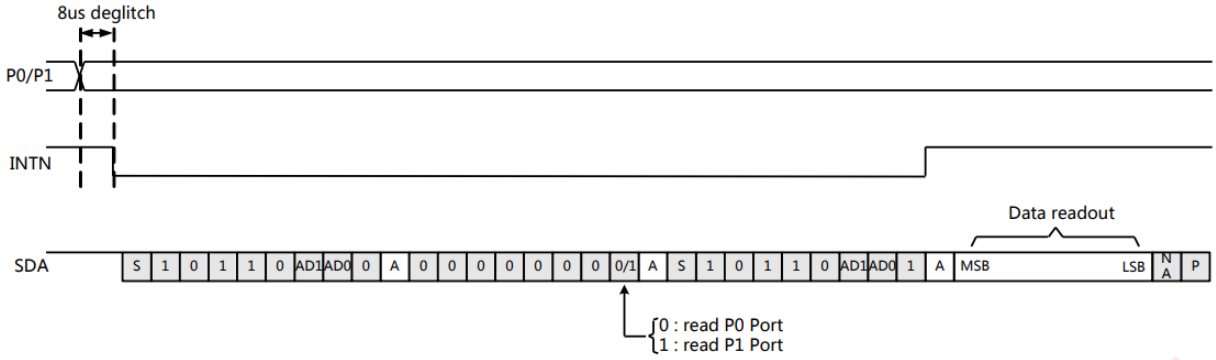


Figure 2 Interrupt generation and clear

6 LED DRIVE

HTR3316B is co-anode current source LED drive. LED drive IMAX is configured by GCR (ISEL) register, to select 4 grades. The default I_{MAX} is 37mA.

In LED drive mode, LED dim step can be manually controlled by external MCU. Drive current is from 0~I_{MAX} divided by 256 steps.

HTR3316B 集成了 16 路共阳恒流型 LED 驱动，通过指令可将 12H 和 13H 寄存器把 P0 口和 P1 口配置为 LED 驱动模式。芯片内置电阻设定了驱动电流的最大值（I_{MAX}）为 37mA（典型）。同时，设置 ISEL[1:0]可将调光范围限定在 0~IMAX、0~(IMAX × 3/4)、0~(IMAX×2/4)或 0~(IMAX×1/4)四个不同区间内，ISEL[1:0]配置方式见表 9。

在确定最大驱动电流基础上，每一路 LED 可以通过 DIM 寄存器进行 256 步线性调光。DIMx（x=0~3）字长 8bits，具体的调光等级见表 2。HTR3316B 对低 6 路 LED 驱动的 Dropout 性能做了强化，仅需 60mV 的电流源压降就可提供 20mA 的 LED 电流，使其更适合驱动 LCD 背光。在驱动 LCD 背光时建议选取这几路。

Table2 256 steps dimming

DIMx bit								D
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	1/255×I_{MAX}
0	0	0	0	0	0	1	0	2/255×I_{MAX}
……								……
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

7 I2C INTERFACE

HTR3316B support I^2C interface. The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

HTR3316B 通过 I^2C 接口与 MCU 通信，支持两种模式：标准模式（100kHz），和快速模式（400kHz）。HTR3316B 作为从机连接在 I^2C 网络上。SCL 为单向输入口；SDA 为双向输入/输出口。当 SDA 做输出时，为开漏输出模式，需外接上拉电阻。在 SCL 线是高电平时，SDA 线从高电平向低电平切换则表示 I2C 接口的起始条件。所有的传输均开始于起始条件或重复起始条件。在 SCL 线是高电平时，SDA 线从低电平向高电平切换则表示 I^2C 接口的停止条件。

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (AD1/AD0) of the slave device must not be changed between the Start and Stop conditions.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

On the I2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remainstable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

所有的传输都被停止条件或重复起始条件所终止。

在起始条件产生之后，I2C 总线将发送一个从机的地址。当 HTR3316B 识别了起始条件之后，会等待接收从机地址。如果 SDA 线上发送的地址与某一从机地址相同，则该从机器件将 SDA 线拉低以响应（应答）。

当时钟线（SCL）为高电平时，SDA 线上的数据必须保持稳定。除了起始条件和停止条件以

外，SDA 线上的电平必须只能在 SCL 为低时才能改变。

应答用于表示数据的成功传送。当发送方（主机）发送了 8bits 数据之后，必须释放 SDA 线。接收方（从机）在应答时钟脉冲期间，必须拉低 SDA 线。HTR3316B 在每接收一字节数据之后会产生一个应答。

在读模式下，从机 HTR3316B 先发送 8 位数据，然后释放 SDA 线并检测 SDA 线上的应答。如果检测到应答，且主机没有发送停止条件，则从机将继续发送数据。如果未检测到应答，则从机将停止发送数据并等待停止条件。

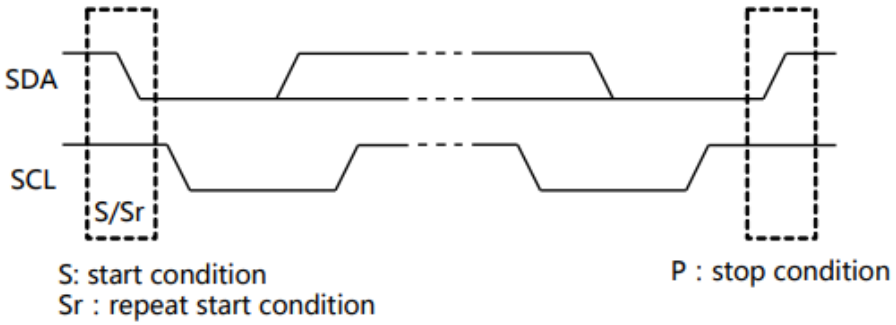


Figure 3 I2C Start and stop condition

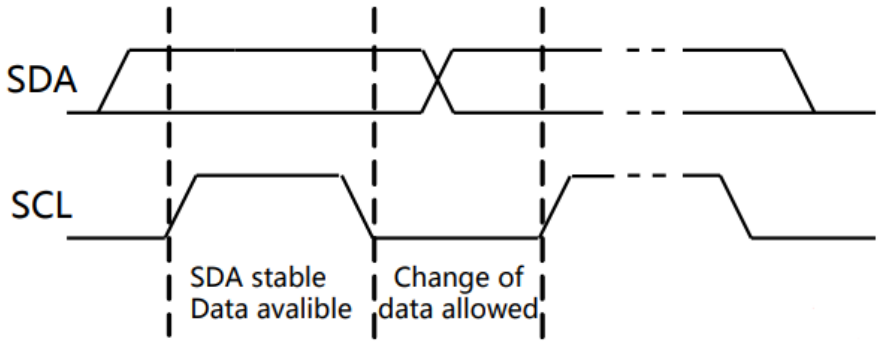


Figure 4 I2C Bit Transfer

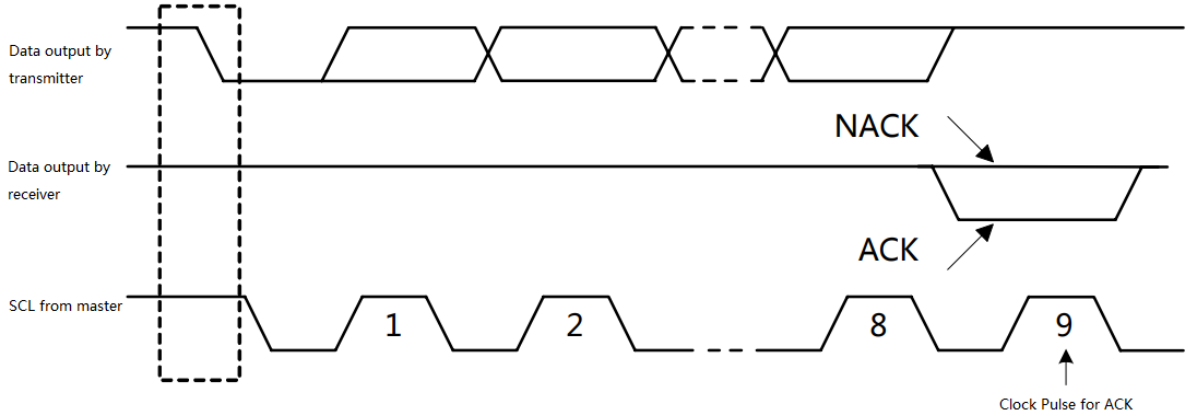


Figure 5 Acknowledgment On I2C Bus

8 DEVICE ADDRESS

Below is the device address of HTR3316B. AD1/AD0 bit in device address match with AD1/AD0 pin respectively.

HTR3316B 提供 2 bits 地址引脚 AD1、AD0，这允许一个 I2C 总线最多可同时使用 4 个 HTR3316B 器件。由 7 位从机地址加一位读写判断位（R/W ）组成了 8 位地址，它在起始条件之后被首先传输。如果所传输的从机地址与总线上的某一个器件地址相符合，则被寻址的接收方将 SDA 线拉低（应答）。

从机地址的高五位固定为“10110”。第六、七位依次是 AD1、AD0，其值由硬件引脚 AD1、AD0 的值决定。第八位（LSB）是读写标志位，它定义了接下来的操作是读或写操作。‘1’表示读，‘0’表示写。

1	0	1	1	0	AD1	AD0	R/W

AD1/AD0 value should match with HTR3316B pin AD1/AD0 respectively. AD1、AD0 的值必须与 AD1、AD0 引脚的值一致

Figure 6 Acknowledgment On I2C Bus

9 I2C WRITE

Data is transmitted to the HTR3316B by sending the device address and setting the least-significant bit to a logic 0. The register address byte is sent after the device address and determines which register receives the data that follows the command byte.

After sending data to one register, the next data byte is sent to the other register. There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

如图 7 为 HTR3316B 写操作时序图。主机先发送起始条件，接着发送 7 位从机地址加一位读写位‘0’；当发送的从机地址与某一个 HTR3316B 器件地址相符合时，该 HTR3316B 应答；接着，主机发送 8 位 HTR3316B 寄存器地址，发送的格式为高有效位（MSB）先发送，低有效位（LSB）后发送；HTR3316B 应答后，主机接着发送 8 位寄存器数据，仍然是 MSB 先发送，LSB 后发送。接着，HTR3316B 应答；主机发送停止条件以结束本次传输。

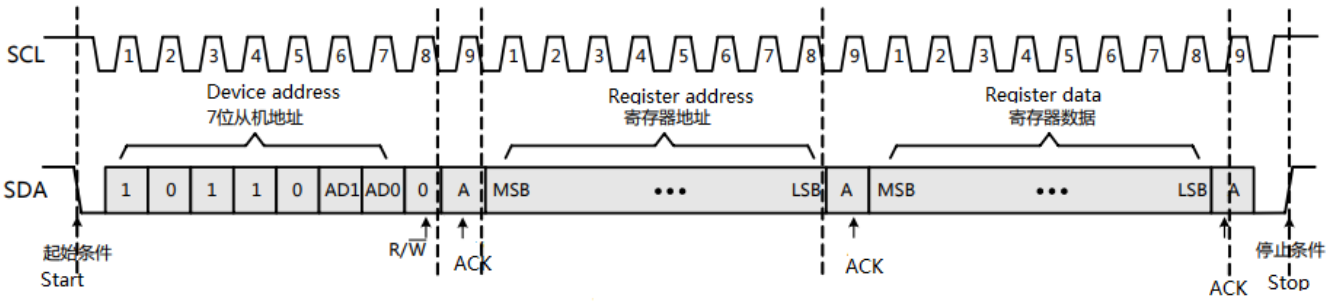


Figure 7 I2C Write operation

10 I2C READ

The bus master first must send the HTR3316B address with the least-significant bit set to a logic 0. The register address byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the register address byte then is sent by the HTR3316B.

After a restart, the value of the register defined by the register address byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

如图 8 为 HTR3316B 读操作时序图。主机先发送起始条件，接着发送 7 位从机地址加一位读写位‘0’；当发送的从机地址与某一个 HTR3316B 器件地址相符合时，该 HTR3316B 应答；接着，主机发送 8 位 HTR3316B 寄存器地址，发送的格式为高有效位（MSB）先发送，低有效位（LSB）后发送，且 HTR3316B 应答；然后，主机发送停止条件及重复起始条件，接着发送 7 位从机地址加一位读写位‘1’，HTR3316B 应答；应答之后，HTR3316B 发送 8 位寄存器数据，发送的格式仍为 MSB 在前，LSB 在后；在接下来的应答时钟，主机不应答，接着主机发送停止条件以结束本次传输。

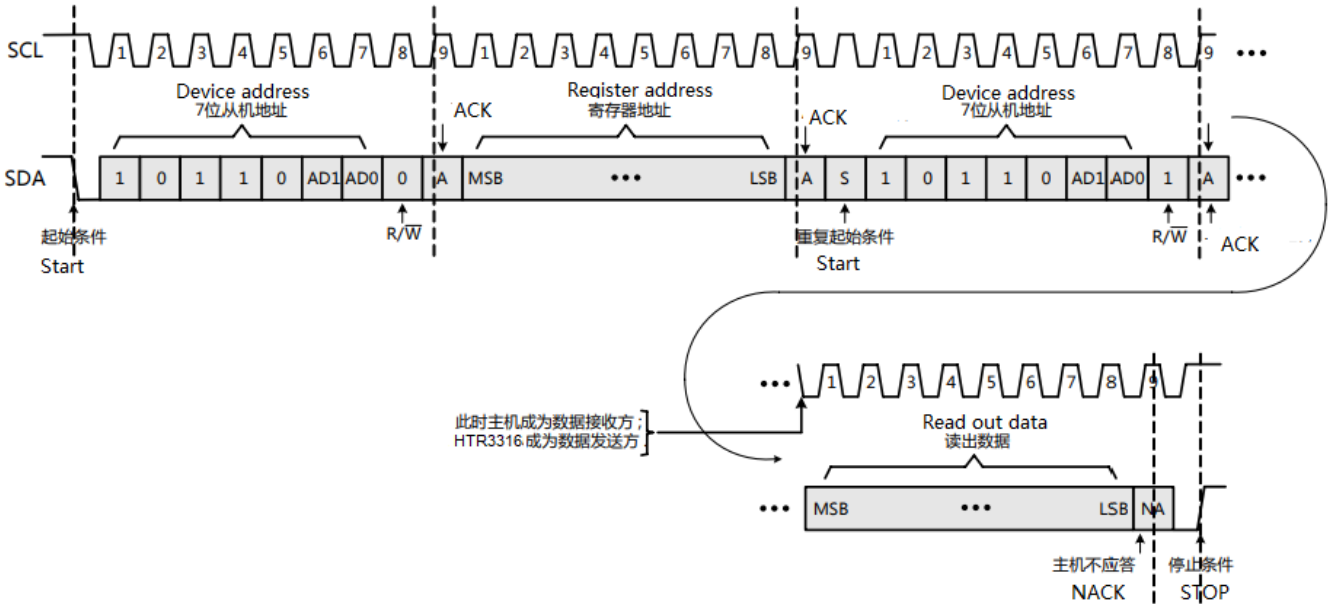


Figure 8 I²C Read operation

11 I2C READ

HTR3316B support 3 reset mode: power on reset, hardware reset, software reset. Each reset mode can reset registers to default value.

HTR3316B 支持三种复位模式：上电复位、硬件复位和软复位。三种复位模式均能将寄存器复位至默认值。

HARDWARE RESET

硬件复位

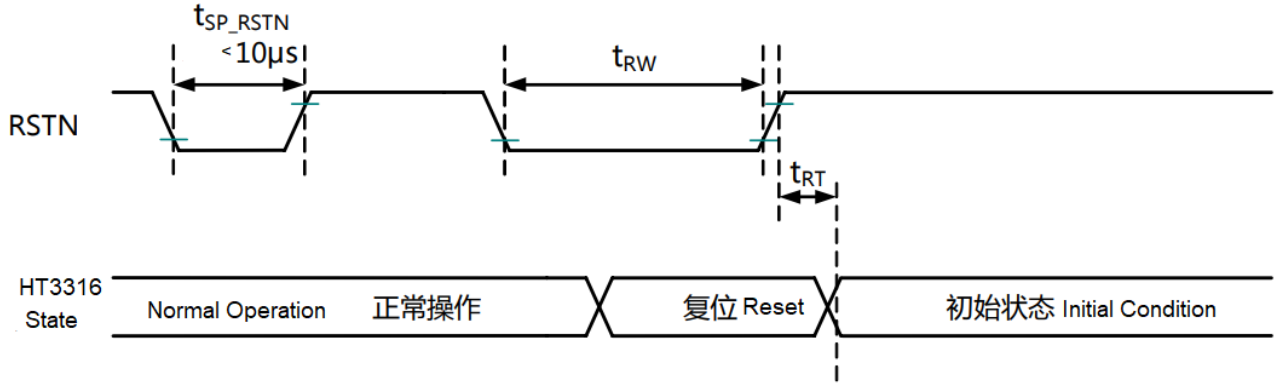


Figure 9 Hardware Reset Timing

Table3 Hardware Reset Parameter

Parameter		Condition	min	typ	max	unit
t_{RW}	Reset pulse low level width	VSS=0V，VCC=2.4V~5.5V，T=-40℃~125℃	20			us
t_{RT}	Reset recovery time		1			us

NOTE:

1. The hardware reset PIN（RSTN）has a built-in deglitch block. Spike due to an electrostatic discharge on RSTN line does not cause irregular system reset.

注意：

1.硬件复位引脚（RSTN）内置了防抖动电路。由静电放电（ESD）或其他干扰而引起的尖峰脉冲，不会引起系统的复位。

2. After reset, HTR3316B is in default state. All GPIO are configured as output, which value is decided by 2 device address (AD1/AD0) (refer to table 1). The interrupt (INTN) is cleared and pulled up by external pull-up resistor.
3. Spike Rejection also applies during a valid reset pulse as shown below:

注意：

2. 复位后，HTR3316B 处于默认状态。此时所有 GPIO 口被配置为输出，其输出值由 2 位器件地址（AD1、AD0）决定，具体值参考表 1；中断状态（INTN）被清除，由外部上拉电阻将其拉高。
3. 在复位脉冲的低电平期间，防抖动电路也将起作用，小于 10ns 的高脉冲将被滤除，如图所示：

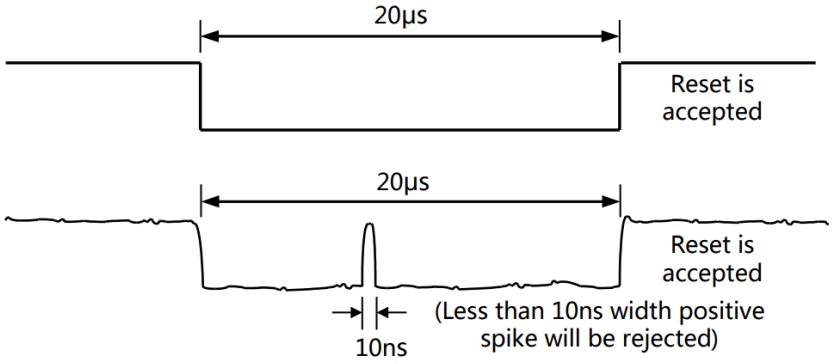


Figure 10 Operation When RSTN IS LOW

12 SOFTWARE RESET

HTR3316B support software reset mode. Writing 00H to the software register(7FH) will generate a reset pulse. After software reset, HTR3316B is in default state, which is the same as hardware reset. The software reset timing is as below. After the software reset command is send through the I2C interface, it takes at least 1ms for chip to acknowledge the new I2C command.

HTR3316B 同时支持软复位模式。每次通过 I2C 接口对软复位寄存器（7FH）写数据 00H，则会产生一次复位脉冲。软复位后，HTR3316B 处于默认状态，其状态与硬件复位相同。软复位时序如图所示。

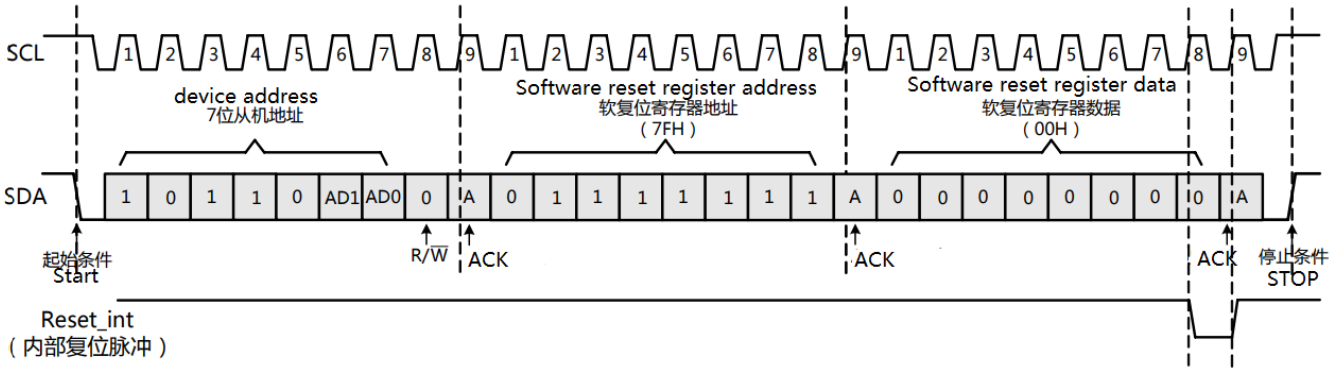


Figure 11 Software Reset Timing

13 Register Map

Table4 Register Map

Register Address	R/W	Name	Function	Default Value
00h	R	Input_Port0	P0 port input state	Equal to P0
01h	R	Input_Port1	P1 port input state	Equal to P1
02hj	R	Output_Port0	P0 port output state	Refer to table 1
03h	R/W	Output_Port1	P1 port output state	Refer to table 1
04h	R/W	Config_Port0	P0 port direction configure	00h
05h	R/W	Config_Port1	P1 port direction configure	00h
06h	R/W	Int_Port0	P0 port interrupt enable	00h
07h	R/W	Int_Port1	P1 port interrupt enable	00h
10h	R	ID	ID register (read only)	23h
11h	R/W	CTL	Global control register	00h
12h	R/W	LED Mode Switch	P0 port mode configure	FFh
13h	R/W	LED Mode Switch	P1 port mode configure	FFh
20h	W	DIM0	P1_0 LED current control	00h
21h	W	DIM1	P1_1 LED current control	00h
22h	W	DIM2	P1_2 LED current control	00h
23h	W	DIM3	P1_3 LED current control	00h
24h	W	DIM4	P0_0 LED current control	00h
25h	W	DIM5	P0_1 LED current control	00h
26h	W	DIM6	P0_2 LED current control	00h
27h	W	DIM7	P0_3 LED current control	00h
28h	W	DIM8	P0_4 LED current control	00h
29h	W	DIM9	P0_5 LED current control	00h
2Ah	W	DIM10	P0_6 LED current control	00h
2Bh	W	DIM11	P0_7 LED current control	00h
2Ch	W	DIM12	P1_4 LED current control	00h
2Dh	W	DIM13	P1_5 LED current control	00h
2Eh	W	DIM14	P1_6 LED current control	00h
2Fh	W	DIM15	P1_7 LED current control	00h
7Fh	W	SW_RSTN	Software reset	00h
other	-	-	Reserved, user should not write these registers, or may cause function error	-

Register Address: 00h, 01h, Input state register (default Equal to P0, P1)

Address	Name	Default	Description
00h	Input_Port0	x	P0 port current logic state, 0-low level；1-high level P0 口引脚当前逻辑状态。0-低电平；1-高电平
01h	Input_Port1	x	P1 port current logic state, 0-low level；1-high level P1 口引脚当前逻辑状态。0-低电平；1-高电平

The Input state registers (00H,01H) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I2C device know that the Input Port registers will be accessed next.

输入状态寄存器（00H，01H）用以反映GPIO口当前的逻辑状态，不论该 GPIO 口是配置为输入模式还是输出模式。该寄存器仅支持读操作；写操作无效。其默认值由外部引脚电平决定。

通过I2C接口读取00H的值，可以清除由 P0 口引起的中断；读取 01H 的值，可以清除由 P1口引起的中断。在读操作之前，必须先通过 I2C接口写入待读取的寄存器地址。

寄存器 00H 的第 7 至第 0 位依次对应 P0_7~P0_0 的输入状态，01H 的第 7 至第 0 位依次对应 P1_7~P1_0 的输入状态。

Register Address: 02h, 03h, Output state register (default Refer to Table1)

Address	Name	Default	Description
02h	Output_Port0	Refer to Table1	Set P0 port output value. 0-low level; 1-high level 设置 P0 口引脚输出值。0-输出低电平；1-输出高电平
03h	Output_Port1	Refer to Table1	Set P1 port output value. 0-low level; 1-high level 设置 P1 口引脚输出值。0-输出低电平；1-输出高电平

The Output state register（02H, 03H）show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

输出状态寄存器（02H，03H）用以设置 GPIO 口的输出值。对于配置为输入模式的 GPIO 口，其对应的位无效；同样地，读取该寄存器的值也只能读到寄存器本身的值，而不能读到对应端口上的状态。

寄存器 02H 的第 7 至第 0 位依次对应 P0_7~P0_0 的输出状态，03H 的第 7 至第 0 位依次对应 P1_7~P1_0 的输出状态。

Register Address: 04h, 05h, Configuration register (default 00h)

Address	Name	Default	Description
04h	Config_Port0	00h	P0 port input/output mode select. 0-output; 1-input P0 口输入/输出模式选择。0-输出模式；1-输入模式
05h	Config_Port1	00h	P1 port input/output mode select. 0-output; 1-inputl P1 口输入/输出模式选择。0-输出模式；1-输入模式

The Configuration registers (04H, 05H) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

配置寄存器（04H，05H）用以设置 GPIO 口处于输入模式或输出模式。每一位 GPIO 口可单独配置为输入或输出模式。若某一位设置为 1，则其对应的端口被配置为输入模式；若某一位设置为 0，则其对应的端口被配置为输出模式。

寄存器 04H 的第 7 至第 0 位依次对应 P0_7~P0_0 的配置控制，05H 的第 7 至第 0 位依次对应 P1_7~P1_0 的配置控制。

Register Address: 06h, 07h, Interrupt enable register (default 00h)

Address	Name	Default	Description
06h	Int_Port0	00h	P0 port interrupt enable. 0-enable; 1-disable P0 口中断使能。0-中断使能；1-中断不使能
07h	Int_Port1	00h	P1 port interrupt enable. 0-enable; 1-disable P1 口中断使能。0-中断使能；1-中断不使能

The Interrupt enable register (06H，07H) are used to configure the interrupt enable or disable of GPIO. If a bit in this register is set to 1, the interrupt function of the corresponding port pin is disabled. If a bit in this register is cleared to 0, the interrupt function of corresponding port pin is enabled.

中断使能寄存器（05H，06H）用以设置 GPIO 口的中断使能。若某一位设置为 0，则使能其对应端口的中断功能；若某一位设置为 1，则关闭其对应端口的中断功能。

Register Address: 10h, ID register (default 23h)

Address	Name	Default	Description
10h	ID	23h	ID register, read only, the readout value is 23H ID 寄存器，只读，读出值为 23H

Register Address: 11h, Global control register (GCR) (default 00h)

Bit	Name	Default	Description
D7:D5	Reserved	00	-
D4	GPOMD	0	Set P0 port GPIO output drive mode。设置 P0 口驱动模式 0, P0 port is Open-Drain mode; P0 口为 Open-Drain 1, P0 port is Push-Pull mode P0 口为 Push-Pull 模式
D3:D2	Reserved	00	-
D1:D0	ISEL	00	256 step dimming range select. 256 步调光范围选择 00：0~I_{MAX} 01：0~(I_{MAX}×3/4) 10：0~(I_{MAX}×2/4) 11：0~(I_{MAX}×1/4)

D[4] is used to configure P0 port output drive as Open-Drain or Push-Pull mode。 When P0 port use as output with Open-Drain mode, it needs pull-up resistor. If in Push-pull mode, it needs no pull-up resistor.

D1:D0 is used to configure the max drive current of LED。 HTR3316B set max current IMAX to 37mA(typical) default, and through register ISEL[1:0] can set to I_{MAX}×1/4, I_{MAX}×2/4, I_{MAX}×3/4,I_{MAX},so the 256 step dimming

range changes.

Except D4, D1:D0, other bits (D7:D5], D3:D2) are used for test purpose and the default value is 0. If user needs to configure register 11H, then the bits D7:D5], D3:D2 must configure to 0, or system function error may occur.

D[4]用以配置 P0 输出模式为开漏（Open-Drain）或推挽（Push-Pull）模式。当 P0 口用做输出时，若使用开漏模式，须外接上拉电阻；若使用推挽模式，则不需上拉电阻。

D1:D0用以配置 LED 驱动的最大电流。默认情况下，芯片内置电阻将最大电流设置为 37mA（典型值），通过 ISEL[1:0]可将该值进一步设定为 I_{MAX}×1/4、I_{MAX}×2/4、 I_{MAX}×3/4、I_{MAX}，从而 256 步调光的范围也随之改变。

该寄存器除D4、D1:D0可配置外，其他位（D7:5D、D3:D2]）为测试使用，默认值为 0；用户若需对寄存器 11H 进行配置，则其 D7:5D、D3:D2必须配置为 0，否则可能引起系统功能错误。

Register Address: 12h, LED mode switch register (default FFh)

Address	Name	Default	Description
12h	LED mode switch	FFh	Configure P0_7~P0_0 as LED or GPIO mode. 配置 P0_7~P0_0 为 LED 或 GPIO 模式 1: GPIO; 0: LED

Register Address: 13h, LED mode switch register (default FFh)

Address	Name	Default	Description
13h	LED mode switch	FFh	Configure P1_7~P1_0 as LED or GPIO mode. 配置 P0_7~P0_0 为 LED 或 GPIO 模式 1: GPIO; 0: LED

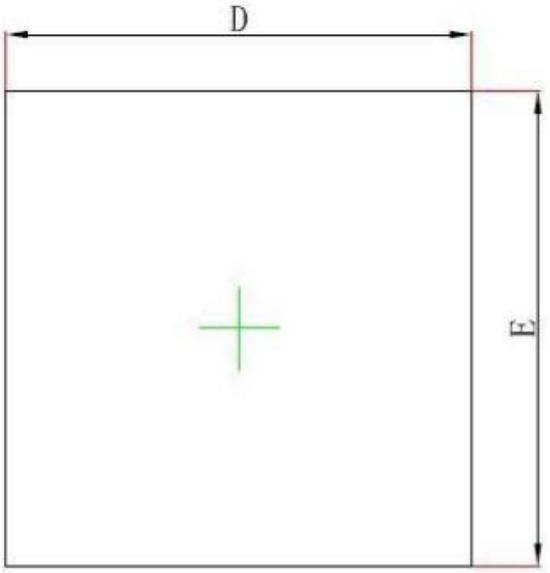
Register Address: 20h~2Fh, 256 step dimming control register (default 00h)

Address	Name	Default	Description
2xh	DIMx	00h	Px_x port LED current control, See Table 4 and table 2.

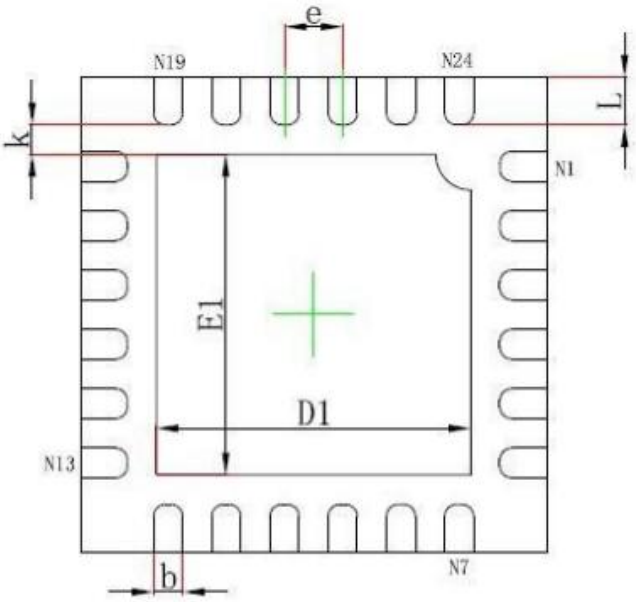
Register Address: 7Fh, Software reset register (default 00h)

Address	Name	Default	Description
7Fh	Software reset	00h	Write 00H to generate a reset pulse, see figure 11. 写 00H 则产生复位脉冲，见图 11.

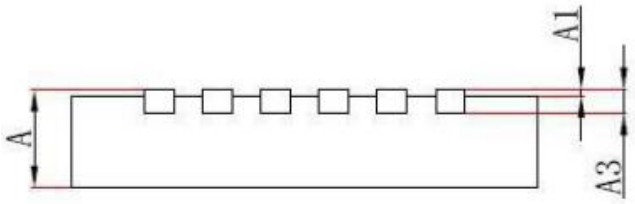
■ PACKAGE OUTLINE



Top View



Bottom View



Side View

Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
A	0.700	0.750	0.800
A1	0.000		0.050
A3	0.195	0.203	0.211
D	3.900	4.000	4.100
E	3.900	4.000	4.100
E1	2.500		2.700
D1	2.600	2.700	2.800
k	0.250MIN.		
b	0.200	0.250	0.300
e	0.500TYP.		
L	0.300	0.400	0.500